

PATENT APPLICATION

#4
3-7-3
Roberts
Electron

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of

Docket No: Q67357

Shinya WATANABE, et al.

Appln. No.: 10/067,320

Group Art Unit: 2818

Confirmation No.: 4591

Examiner: Gene Nghia AUDUONG

Filed: February 7, 2002

For: SEMICONDUCTOR CHIP HAVING AN ARRAYED WAVEGUIDE GRATING AND
METHOD OF MANUFACTURING THE SEMICONDUCTOR CHIP AND MODULE
CONTAINING THE SEMICONDUCTOR CHIP

RECEIVED
FEB 28 2003
TECHNOLOGY CENTER 2800

RESPONSE TO RESTRICTION REQUIREMENT

Commissioner for Patents
Washington, D.C. 20231

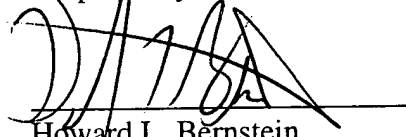
Sir:

In response to the restriction requirement, dated January 29, 2003, Applicant elects
Group I, claims 1-27 for examination. This election is made without traverse.

Applicant reserves the right to file a Divisional Application directed to non-elected
claims 28-36.

The USPTO is directed and authorized to charge all required fees, except for the Issue
Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any
overpayments to said Deposit Account.

Respectfully submitted,


Howard L. Bernstein
Registration No. 25,665

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WASHINGTON OFFICE



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PATENT TRADEMARK OFFICE

Date: February 27, 2003